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SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: **01-286443** [JP 1286443 A]
PUBLISHED: November 17, 1989 (19891117)
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APPL. NO.: 63-116557 [JP 88116557]
FILED: May 13, 1988 (19880513)
INTL CLASS: [4] H01L-021/88; H01L-021/302
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JOURNAL: Section: E, Section No. 885, Vol. 14, No. 67, Pg. 49, February 07, 1990 (19900207)

ABSTRACT

PURPOSE: To uniformize the etching time of wiring connection holes whose depths are different with each other, at the time of forming the wiring connection holes, improve the connection yield of the wiring connection holes, and prevent the irregularity in pattern conversion difference, by a method wherein an insulating layer is formed by stacking a first insulating layer and a second insulating layer whose etching rates are different, and the thickness of the second insulating film on a conducting layer whose surface is high, is made thinner than the thickness of the second insulating film on a conducting film whose surface is low.

CONSTITUTION: The main surface 10 gas a step-difference whose height is H10. A wiring 6 and a wiring 7 are formed on the main surface 10; an interlayer insulating film 2 is formed; an interlayer insulating film 20 whose material is different from that of the film 2 is formed; the surface of the interlayer insulating film 20 is flattened by, e.g., etching method,

and a surface 3 is obtained; holes 12, 13 for forming wiring connection holes are formed by photo resist 11; the interlayer insulating film 20 is etched at a etching rate a20 by e.g., RIE using the photo resist 11 as a mask; at this time, the etching rate of the interlayer insulating film 2 is set as a2.

English Translation of JP01-286443

(19) Japanese Patent Office (JP)

(11) Publication Number: Hei 01-286443

(43) Date of publication of application: November 17th, 1989

(12) Patent Laid-open Official Gazette (A)

(51) Int. Cl.[4]

H01L 21/88

H01L 21/302

The Number of Invention: 3 (8 pages in total)

Request of Examination: not made

(54) Title of Invention: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

(21)Application Number: Sho 63-116557

(22) Filing Date: May 13th, 1988

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Specification

1. [Title of the Invention]

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

2. [Scope of Claims]

[Claim 1] A semiconductor device comprising a conductive layer including a step on a surface of a semiconductor substrate where electrode wirings are formed; and an insulating layer in which a predetermined portion is opened over the conductive layer, wherein the insulating layer is formed by stacking first and second insulating layers of which etching rates are different, a thickness of the second insulating layer over a conductive layer where a height of a surface is high is thinner than that of a second insulating film over a conductive layer where a height of a surface is low.

[Claim 2] A manufacturing method of the semiconductor device according to claim 1, wherein a wiring connection hole is formed by an etching method using a photo resist as a mask in which an etching rate of the second insulating layer is higher than that of the first insulating layer.

[Claim 3] A manufacturing method of the semiconductor device according to claim 1 comprising a first step for dry etching an insulating film layer by using a photo resist as a mask; and a second step for etching the photo resist

and the insulating film layer simultaneously using a dry etching method in which an etching rate of the photo resist is higher than that of the insulating film layer.

3. [Detailed Description of the Invention]

[Industrial Field for the Invention]

The present invention relates to a semiconductor device and a manufacturing method thereof, and more concretely to a structure of a wiring connection hole in a multilevel interconnection of an integrated circuit and a forming method thereof.

[Prior Art]

Figs. 7 (A) and (B) show a forming method of a conventional wiring connection hole. Since planarization of a surface 3 of an interlayer insulating film 2 improves homogenization of transmission characteristics of a wiring and is effective for preventing disconnection of a wiring and a leak current between wirings, it is essential in accordance with miniaturization of a wiring. Since the planarization in a multilevel interconnection is generally performed over a base with unevenness, difference between depths of wiring connection holes 4 and 5 which are formed by etching in aperture portions of a photo resist 11 approaches a height of a step which the unevenness of the base has, as the planarization degree of the surface 3 is improved. Consequently, times required for etching in forming the wiring connection holes 4 and 5 are different, so that an exposed surface 8 on a base 6 of the wiring connection hole 4 which is shallow is exposed in an atmosphere of

etching even after finishing etching of the wiring connection hole 4 until the wiring connection hole 5 which is deep is finished forming. In this case, reference symbol a denotes an etching rate of the interlayer insulating film 2; b denotes that of the base 6; and H4 and H5 respectively denote depths of the wiring connection holes 4 and 5. A depth h6 (see Fig. 7 (B)) which the base 6 is etched at finish of etching is at least

$h6 = b (H5 - H4) / a.$

[Problems to be Solved by the Invention]

Such an etching of the base is not only unnecessary, but also causes a disconnection defect. Besides, pattern conversion difference by etching is easy to increase by being exposed in an atmosphere of etching after finish of etching, so that it is required to make an etching time uniform from a viewpoint of miniaturization of a pattern.

[Means for Solving the Problems]

In view of the foregoing, it is an object of the present invention to provide a wiring connection hole forming method for making an etching time of wiring connection holes having different depths uniform to improve a connection yield of the wiring connection hole and prevent fluctuation of pattern conversion difference in a formation of a wiring connection hole.

Figs. 6 (a) to (f) are principle views for describing a structure and a forming method of a semiconductor device of the present invention in order of steps. A main surface 10 of a substrate 1 has a step with a height of H10 (a).

Wirings 6 and 7 are formed on the main surface 10 (b). After that, an interlayer insulating film 2 is formed (c). Subsequently, an interlayer insulating film 20 of which material is different from the interlayer insulating film 2 is formed. A surface of the interlayer insulating film 20 is planarized by, for example, an etching method, so that a surface 3 is obtained (d). Holes 12 and 13 for forming wiring connection holes are formed by using a photo resist 11 (e). Next, the interlayer insulating film 20 is etched by, for example, a reactive ion etching method (RIE) at an etching rate a20 by using the photo resist 11 as a mask. At this time, the interlayer insulating film 2 is etched at an etching rate a2. A time T6 while the wiring 6 is exposed in an atmosphere of etching until etching of a connection hole 5 is completed is H10/a20. H10 is illustrated in Fig. 6 (a). The higher the etching rate a20, the time T6 becomes shorter. In addition, the higher the etching rate a20 as compared to the etching rate a2, a ratio of T6 to an etching finishing time of the connection hole 5 is reduced so that a wiring connection hole forming time can be made uniform (f). As set forth above, the semiconductor device of the present invention has a structural characteristic that the interlayer insulting film has a two-layer structure, and a film thickness ratio of the interlayer connection film 20 with high etching rate to the interlayer insulating film 2 with low etching rate becomes higher in a position of a wiring connection hole as the wiring connection hole becomes deeper.

[Embodiment]

Fig. 1 is a cross sectional view of a first embodiment of a wiring connection hole forming method of the present invention. In the drawing, reference numeral 1 denotes a substrate formed by integrating a semiconductor device; 2 denotes an insulating film; 20 denotes an insulating film of which material is different from that of 2; 3 denotes a surface of a most upper insulating film; 4 and 5 denote wiring connection holes; 6 and 7 denote wirings; 8 and 9 denote exposed portions of respective wirings 6 and 7; 10 denotes a main surface of the substrate 1; and 11 denotes a photo resist.

Hereinafter, a manufacturing method of a wiring connection hole shown in Fig. 1 is described with reference to Fig. 4.

A step with a height of H10 exists on the main surface 10 of the substrate 1 formed by integrating a semiconductor device such as a MOS field effect transistor or a bipolar transistor, a region for separating elements, or the like. A wiring of which material is, for example, aluminum is formed on the main surface 10 by an aluminum depositing step, a photolithography step and an etching step. The wiring 6 typifies a wiring formed on a higher portion of the step of the main surface 10, and the wiring 7 typifies a wiring formed on a lower portion of the step of the main surface 10. Subsequently, the insulating film 2 of which material is, for example, SiO_2 is deposited. The deposit of SiO_2 can be performed by a vapor phase reaction and sputtering. A film thickness of SiO_2 is required to be enough to deposit the wiring. It is approximately 100 nm with respect to a height of 1 μm of a wiring. Si_3N_4 can be used for the insulating film 2. Next, the insulating film 20 using PSG

as a material is deposited with a film thickness of approximately 1 μm. Subsequently, the surface 3 of the insulating film 20 which is planarized using a surface planarization method such as an etch back method is obtained. For that purpose, for example, an organic polymeric material layer 12 is applied thereover, which is treated thermally to form a wiring structure having a plane surface. Next, the surface of the wiring structure which is structured in this manner is etched by RIE under the condition that etching rates of the insulating film 20 and the organic polymeric material layer 12 are the same, so that the plane surface 3 is obtained by removing a convexity of the insulating film 20 simultaneously with etching of the organic polymeric material layer 12.

Next, after the photo resist 11 is applied with a film thickness of 1.6 μm by the photolithography step, the aperture positions 13 and 14 for the wiring connection holes are exposed by patterning, and the surface 3 is covered with a photo resist.

An etching of the wiring connection hole is performed with a normal RIE apparatus, and an etching rate of PSG is 130 nm/min while that of SiO_2 is 36 nm/min in the case of using CHF_3/O_2 mixed gas as an etching gas at a flow ratio of 9/50 SCCM, at a pressure of 50 mTorr, and at a RF electric power of 1000 W. Here, for example, the step H10 is 0.5 μm, the depth of the wiring connection hole 4 is 0.5 μm, the depth of the wiring connection hole 5 is 1 μm, and the film thickness of the insulating film 2 is 0.5 μm. In this case, the wiring connection hole 4 is overetched for about 3.8 minutes until an etching

of the wiring connection hole 5 is finished. It corresponds to 22% of the total etching time. On the one hand, in the case that SiO_2 is used for all of the interlayer insulating films, the wiring connection hole 4 is overetched in the same way for about 13.9 minutes, which corresponds to 50% of the total etching time. On the other hand, in the case that PSG is used for all of the interlayer insulating films, the overetching time of the wiring connection hole is the same as that of the present embodiment, however, which corresponds to 50% of the total etching time. As set forth above, in the wiring structure in which the main surface 10 of the base has a step and the surface 3 is planarized, the etching finish times of the wiring connection holes having different depths can approach by that the interlayer insulating film is formed to have a two-layer structure and the etching rate of the upper layer is made to be higher than that of the lower layer. As a result, an unnecessary overetching time can be shortened, so that a disconnection defect and increase of pattern conversion difference due to etching of an aluminum wiring accompanied by an overetching can be prevented.

In addition, it goes without saying that the interlayer insulating film 20 can remain over the entire surface after the etch back as shown in Fig. 6.

Fig. 2 is a cross sectional view of a second embodiment of a wiring connection hole forming method of the present invention. It shows the case that wiring connection holes are formed on impurity-dispersed layers 16 and 17, and similarly to the case of the first embodiment, an unnecessary overetching time of the wiring connection hole 4 can be shortened.

Fig. 3 is a cross sectional view of a third embodiment of a wiring connection hole forming method of the present invention.

Hereinafter, a manufacturing method of a wiring connection hole shown in Fig. 3 is described with reference to Fig. 5.

An etching of the wiring connection hole is performed, as a first stage by using CHF_3/O_2 mixed gas as an etching gas at a flow ratio of 9/50 SCCM, at a pressure of 50 mTorr, at a RF electric power of 1000 W, and an etching rate of PSG is 130 nm/min while that of SiO_2 is 36 nm/min. In the first stage, time for which PSG is etched to 0.5 μm and SiO_2 is etched to 0.14 μm is selected. Subsequently, as a second stage, an etching is performed by using CHF_3/O_2 mixed gas as an etching gas at a flow ratio of 75/50 SCCM, at a pressure of 50 mTorr, at a RF electric power of 1000 W, and an etching rate of PSG is 50 nm/min, that of SiO_2 is 20 nm/min, and that of the photo resist 11 is 100 nm/min. As the second stage, time for which SiO_2 is etched to 360 nm and the photo resist is etched to 0.9 μm is selected. At this time, the photo resist is side-etched at 50% of the above-described etching rate and is enlarged to approximately 0.5μm on one side as compared to that when the etching is started. When the etching of the second stage is finished, the wiring connection hole 4 is finished etching so that the exposed surface 8 of the base wiring 6 is exposed. On the other hand, a portion of 0.14 μm which is not etched in the interlayer insulating film 2 remains in the wiring connection hole 5. Succeedingly, as a third stage, the same etching condition as that of the first stage is selected, and SiO_2 is etched to 0.14 μm to expose

an exposed surface 9 of the base wiring 7 so that the etching of the wiring connection hole 5 is completed. A sidewall of the wiring connection hole has inclination accompanied by enlarging the exposed portions 13 and 14 of the photo resist 11 in the second stage, and the hole diameter becomes larger in upper surface of an aperture, so that the wiring connection holes become taper shapes where the exposed surfaces 8 and 9 of the base wirings keep the initial hole diameters. As one effect, the wiring is easy to enter into the connection hole, so that throwing power of wiring is improved, and consequently the yield of connection in the wiring connection hole is improved. As another effect, the exposed diameter of the base wiring is not enlarged, so that an aligning margin of the wiring connection hole and the base wiring is not required to enlarge, and consequently it is favorable for miniaturizing a pitch of wiring.

In the case that SiO_2 is used for all of the interlayer insulating films and the taper shape of the wiring connection hole is obtained in the same way of the second stage in the embodiment 3, if the initial hole diameter in the exposed portion 8 of the base wiring in the wiring connection hole 4 of which depth is shallow is intended to keep, a time schedule in which the second stage can be applied in an etching process of the wiring connection hole is limited, so that the inclination of the sidewall cannot be obtained under 0.5 μm from the upper portion of the wiring connection hole 5 as a shape of the wiring connection hole. Consequently, the improvement for throwing power of wiring has less effect as the hole diameter is miniaturized and the step of

the base becomes large. Besides, it is obvious that the overetching time for the wiring connection hole is longer than that of the present embodiment 2.

In the case that PSG is used for all of the interlayer insulating films and the taper shape of the wiring connection hole is obtained in the same way of the second stage in the embodiment 3, the taper shape cannot be formed in a bottom portion of 0.5 μm of the wiring connection hole 5 as a shape of the wiring connection hole in order to prevent enlarging the hole diameter in the exposed portion 8, and furthermore, there is a practical problem that it is difficult to find a stable etching condition for making an etching rate ratio of a photo resist to PSG high. In the case of a level in the second stage of the embodiment 3, it is not so much expected that the throwing power of wiring is improved since the photo resist is enlarged to 0.2 μm on one side.

Accordingly, in the present invention, the etching time of the wiring connection holes having different depths can be uniform. Besides, a position of the taper of the sidewall in the wiring connection hole can be set freely without changing the pitch of wiring.

[Effects of the invention]

As mentioned above, the overetching time of a wiring connection hole can be shortened according to the present invention. An effect thereof is that a yield of wiring connection is improved since a quantity of etching of a wiring connection hole base accompanied by overetching is reduced. Furthermore, there is an effect that control of a pattern conversion difference

at etching of the wiring connection hole is improved since enlargement of the wiring connection hole by side etching accompanied by overetching is reduced. It is advantageous to miniaturization of a pitch of wiring. An inclination of a sidewall of a wiring connection hole can be controlled in the present invention. Furthermore, a position to enlarge the wiring connection hole can be set freely while keeping a hole diameter of the bottom of the wiring connection hole the initial size in the present invention. As an effect thereof, steepness of the step in the wiring connection hole is eased without reducing a margin for fitting the wiring connection hole, so that throwing power of wiring is improved even in a microscopic wiring connection hole, and consequently the improvement of the yield of wiring connection can be realized.

4. [Brief Description of the Drawings]

Fig. 1, Fig. 2 and Fig. 3 are cross sectional views each showing one embodiment of a semiconductor device of the present invention.

Figs. 4 (a) through (h) are cross sectional views showing one embodiment of a manufacturing method of the semiconductor device shown in Fig. 1 in order of steps.

Figs. 5 (a) through (d) are cross sectional views showing one embodiment of a manufacturing method of the semiconductor device shown in Fig. 3 in order of steps.

Figs. 6 (a) through (f) are cross sectional views showing a structural principle

of the semiconductor device of the present invention in order of steps.

Figs. 7 (A) and (B) are cross sectional views showing one example of a manufacturing method of the conventional semiconductor device in order of steps.

1 ... substrate formed by integrating a semiconductor device

2 ... insulating film

3 ... surface of a most upper insulating film

4, 5 ... wiring connection hole

6, 7 ... wiring

8, 9 ... exposed portion of wirings 6 or 7

10 ... main surface of substrate 1

11 ... photo resist

12 ... organic polymeric material layer

13, 14 ... aperture of wiring connection hole 4 or 5 of photo resist 11

16, 17 ... impurity-dispersed layer

20 ... insulating film of which material is different from insulating film 2

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⑲日本国特許庁(JP)　⑪特許出願公開

⑫公開特許公報(A)　平1−286443

⑤Int.Cl.⁴	識別記号	庁内整理番号	⑬公開　平成1年(1989)11月17日
H 01 L 21/88		K−6824−5F	
21/302		L−8223−5F	

審査請求　未請求　請求項の数 3　(全8頁)

⑭発明の名称　半導体装置とその製造方法

⑳特　願　昭63−116557
㉒出　願　昭63(1988)5月13日

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明　細　書

1.発明の名称

半導体装置とその製造方法

2.特許請求の範囲

(1) 電極配線を形成すべき半導体基板の一表面に表面段差を含む導電層を有し、上記導電層上には所定部分が開孔されてなる絶縁層を有する半導体装置において、上記絶縁層はエッチングレートの異なる第1および第2の絶縁層が積層されてなり、表面の高さが高い導電層上の第2の絶縁層の厚さが表面の高さが低い導電層上の第2の絶縁膜の厚さよりも薄いことを特徴とする半導体装置。

(2) 特許請求の範囲(1)に記載の半導体装置の製造において、ホトレジストをマスクにして上記第2の絶縁層のエッチングレートが第1の絶縁層のエッチングレートより大きいエッチング方法を用いて配線接続穴を形成することを特徴とする半導体装置の製造方法。

(3) 特許請求の範囲(1)に記載の半導体装置の製造において、ホトレジストをマスクにして絶縁膜層をドライエッチングする第1の工程と、該ホトレジストのエッチングレートが上記絶縁膜層のエッチングレートより大きいドライエッチング方法により前記ホトレジストと上記絶縁膜層とを同時にエッチングする第2の工程とを含むことを特徴とする半導体装置の製造方法。

3.発明の詳細な説明

〔産業上の利用分野〕

本発明は、半導体装置とその製造方法に関するものであり、具体的には、集積回路の多層配線における配線接続穴の構造とその形成方法に関する。

〔従来の技術〕

第7図(A),(B)は、従来の配線接続穴の形成方法を示したものである。層間絶縁膜2の表面3の平坦化は配線の伝達特性の均質化を向上させ、

配線の断線および線間の漏れ電流防止に有効なことから、配線の微細化に伴い必須となつている。一般に多層配線における平坦化は凹凸のある下地上になされるため、表面３の平坦度が向上する程、ホトレジスト１１の開口部にエッチングによつて形成される配線接続穴４および５の穴の深さの差は下地の凹凸の持つている段差の高さに近づくことになる。このため配線接続穴４と５を形成する際のエッチングに必要な時間が異なり、浅い方の配線接続穴４の下地６の露出面８は、配線接続穴４のエッチングが完了した後も、深い方の配線接続穴５の形成が完了するまでエッチング雰囲気にさらされることになる。この場合、層間絶縁膜２のエッチングレートをａ、下地６のエッチングレートをｂとし、配線接続穴４および５の深さをそれぞれＨ４、Ｈ５とする。エッチング完了時に下地６がエッチングされる深さｈ６（第７図（Ｂ）参照）は少なくとも

ｈ６＝ｂ（Ｈ５－Ｈ４）／ａとなる。

〔発明が解決しようとする課題〕

こうした下地のエッチングは不必要なばかりでなく、配線不良の原因にもなる。また、エッチングによるパタン変換差はエッチング完了後にエッチング雰囲気にさらされることにより増加しやすいので、パタンの微細化の観点からもエッチング時間の均一化が必要である。

〔課題を解決するための手段〕

本発明の目的は、配線接続穴の形成において、異なる深さの配線接続穴のエッチング時間を均一化し、配線接続穴の接続歩留りの向上とパタン変換差のばらつきを防止した配線接続穴形成方法を提供することにある。

第６図(a)～(f)は、本発明による半導体装置の構造とその形成方法を工程順に説明するための原理図である。基板１の主面１０は高さＨ１０の段差を有する(a)。主面１０上に配線６および配線７を形成する(b)。その後、層間絶縁膜２を形成する(c)。続いて層間絶縁膜２と材料の異なる層間絶縁膜２０を形成する。層間絶縁膜２０の表面は例えばエッチング法により平坦化し表面３を得る(d)。ホトレジスト１１により配線接続穴形成用の穴１２および１３を形成する(e)。次に、例えばリアクティブ イオン エッチング法（ＲＩＥ）によりホトレジスト１１をマスクにして層間絶縁膜２０をエッチングレートａ２０でエッチングする。この時、層間絶縁膜２のエッチングレートはａ２とする。接続穴５のエッチング完了までに配線６がエッチング雰囲気にさらされる時間Ｔ６はＨ１０／ａ２０となる。Ｈ１０は第６図(a)を参照されたい。ａ２０が大きい程、Ｔ６も小さくなる。また、ａ２に対してａ２０が大きい程、接続穴５のエッチング完了時間に対するＴ６の割合は減少し配線接続穴形成時間の均一化がはかれる(f)。このように、本発明による半導体装置では層間絶縁膜は２層構造になつており、深い配線接続穴になる程その配線接続穴の位置におけるエッチングレートの大きい層間接続膜２０のエッチングレートの小さい層間絶縁膜２に対する膜厚比率が大きくなるという構造上の特徴を有している。

〔実施例〕

第１図は、本発明による配線接続穴形成方法の第１の実施例を示す断面図である。図において１は半導体デバイスを集積してなる基板、２は絶縁膜、２０は２と材質の異なる絶縁膜、３は最上部絶縁膜の表面、４および５は配線接続穴、６および７は配線、８および９はそれぞれ配線６および７の露出部分、１０は基板１の主面、１１はホトレジストである。

以下、第１図に示した配線接続穴の製造方法を第４図を用いて説明する。

半導体装置デバイス、たとえばＭＯＳ電界効果トランジスタやバイポーラトランジスタおよび素子間分離領域等を集積してなる基板１の主面１０には高さＨ１０の段差が存在する。主面１０上に例えばアルミニウムを材料とした配線をアルミニウム堆積工程とホトリソグラフィ工程とエッチング工程により形成する。配線６は主面１０の段差

の高い法に形成された配線を代表し、配線7は主面10の段差の低い方に形成された配線を代表する。次に、たとえばSiO₂を材料とした絶縁膜2を被着する。SiO₂の被着は気相反応によつて、スパッタリングによつても可能である。SiO₂の膜厚は上記配線を被着できる膜厚であればよく、配線の高さ1μmにたいして100nm程度でよい。絶縁膜2としてはSi₃N₄でもよい。続いて、PSGを材料とした絶縁膜20を1μm程度の膜厚で被着する。続いて、エッチバック法等の表面平坦化法により平坦化された絶縁膜20の表面3を得る。そのため、たとえばこの上に有機高分子材層12を塗布し、これを熱処理して平坦な表面を有する配線構造体を形成する。次に、このように構成された配線構造体の表面をRIEによつて絶縁膜20と有機高分子材層12のエッチングレートが同一となる条件でエッチングし、絶縁膜20の凸部を有機高分子材層12のエッチングと同時に除去して平坦面3を得る。

次に、ホトリソグラフィ工程によりホトレジスト11を膜厚1.6μmにて塗布後、パターニングして配線接続穴の開口位置13および14を露出して表面3上をホトレジストで被覆する。

配線接続穴のエッチングは、通常のRIE装置を用い、エッチングガスにCHF₃/O₂混合ガスを流量比9/50SCCM、圧力50mTorr、RF電力1000W印加した場合には、PSGのエッチングレートは130nm/分、SiO₂のエッチレートは36nm/分である。今、例として段差H10を0.5μm、配線接続穴4の深さを0.5μm、配線接続穴5の深さを1μm、絶縁膜2の膜厚を0.5μmとする。この場合、配線接続穴5のエッチングを終了するまでに配線接続穴4は約3.8分のオーバーエッチングをうける。これは全エッチング時間の22%である。一方、層間絶縁膜としてすべてSiO₂とした場合、配線接続穴4は同様のオーバーエッチングを約13.9分受けることになり、これは全エッチング時間の50%である。また、層間絶縁膜としてすべてPSGとした場合、配線接続穴のオーバーエッチング時間は本実施例と同じであるが、これは全エッチング時間の50%である。この様に、層間絶縁膜を2層構造とし、上層のエッチングレートを下層のエッチングレートより大きくすることにより、下地主面10に段差を持ち表面3の平坦な配線構造体では、深さの異なる配線接続穴のエッチング完了時間を近付けることができる。その結果、不必要なオーバーエッチング時間の短縮ができるので、オーバーエッチングに伴うアルミニウム配線のエッチングによる配線の接続不良やパタン変換差の増加を防止できる。

なお、層間絶縁膜20は第6図のごとくエッチバック後に全面的に表面に残つてもよいことは言うまでもない。

第2図は、本発明による配線接続穴形成方法の第2の実施例を示す断面図である。配線接続穴が不純物拡散層16および17上に形成されてなる場合であり、第1の実施例の場合と同様に、配線接続穴4の不必要なオーバーエッチング時間が短縮できる。

第3図は、本発明による配線接続穴形成方法の第3の実施例を示す断面図である。

以下、第3図に示した配線接続穴の製造方法を第5図を用いて説明する。

配線接続穴のエッチングは、第1段階としてエッチングガスにCHF₃/O₂混合ガスを流量比9/50SCCM、圧力50mTorr、RF電力1000W印加し、PSGのエッチングレートは130nm/分、SiO₂のエッチングレートは36nm/分である。第1段階ではPSGを0.5μmエッチングし、SiO₂を0.14μmエッチングする時間に選ぶ。続いて、第2段階としてエッチングガスにCHF₃/O₂混合ガスを流量比75/50SCCM、圧力50mTorr、RF電力1000W印加し、PSGのエッチングレートは50nm/分、SiO₂のエッチングレートは20nm/ 分、ホトレジスト11のエッチングレートは100nm/分である。第2段階としてSiO₂を360nmエッチングし、ホトレジストを0.9μmエッチングする時間を選ぶ。

この時、ホトレジストは上記エッチングレートの約５０％のサイドエッチングを受けて、エッチング開始時より片側約０．５μｍ拡大する。第２段階のエッチング終了時に配線接続穴４はエッチングを完了して下地配線６の露出面８があらわれる。一方、配線接続穴５には層間絶縁膜２に０．１４μｍの未エッチング部分がある。引続き、第３段階として第１段階と同じエッチング条件に選びＳｉＯ２を０．１４μｍエッチングし下地配線７の露出面９をあらわして配線接続穴５のエッチングを完了する。第２段階ではホトレジスト１１の露出部分１３および１４の拡大にともなつて配線接続穴の側壁が傾きを持ち、穴径は開口部の上部程大きく下地配線の露出部８、９では初期の穴径を保つテーパ形状となる。その効果としては、配線接続穴に配線が入り込み易くなり配線の付回りが改善されるので、配線接続穴での接続歩留りが改善される。また一つの効果としては、下地配線の露出径は拡大しないので配線接続穴と下地配線との位置合わせマージンを大きくする必要がないので配線ピッチの微細化に有利である。

層間絶縁膜としてすべてＳｉＯ２として、配線接続穴のテーパ形状を上記実施例３の第２段階と同様の方法で得る場合、深さの浅い方の配線接続穴４の下地配線の露出部８で初期の穴径を保とうとすると、配線接続穴のエッチングプロセスにおいて第２段階の適用できる時間制が限られるので配線接続穴の形状としては配線接続穴５の上部０．５μｍより下に側壁の傾斜は得られない。そのため、配線の付回りの改善は穴径が微細化し、下地段差が大きくなる程、効果がなくなる。また、配線接続穴のオーバーエッチング時間が本実施例２より多くなることも明らかである。

層間絶縁膜としてすべてＰＳＧとして、配線接続穴のテーパ形状を上記実施例３の第２段階と同様の方法で得る場合、露出部８での穴径を拡大防止のためには、配線接続穴の形状として配線接続穴５の下部０．５μｍにはテーパが形成できないばかりでなく、ホトレジストとＰＳＧとのエッチングレート比を大きくする安定したエッチング条件が見いだし難いという実際上の問題がある。実施例３の第２段階における程度の場合、ホトレジストの拡大は片側０．２μｍになるので配線の付回りの改善はほとんど期待できない。

このように、本発明では、異なる深さの配線接続穴のエッチング時間を均一化できる。また、配線接続穴の側壁のテーパの位置を配線ピッチの変更なしで自由に設定できる。

〔発明の効果〕

以上説明したように、本発明では配線接続穴のオーバーエッチング時間の短縮がはかれる。その効果としてはオーバーエッチングに伴う配線接続穴下地のエッチング量が減少するので配線接続歩留りが向上する。さらに効果としてオーバーエッチングに伴うサイドエッチングによる配線接続穴の拡大が減少するので配線接続穴エッチング時のパタン変換差の制御性が向上する。これは配線ピッチの微細化に有利である。本発明では配線接続穴の側壁の傾きを制御できる。さらに本発明では、配線接続穴の最下部の穴径を初期の穴径に保ちながら配線接続穴の拡大する位置を自由に設定できる。その効果としては配線接続穴の合わせマージンの減少を招くことなく、配線接続穴における段差の急峻さが緩和されることになり、微細な配線接続穴にいたるまで配線のつきまわりが改善される結果、配線接続歩留りの向上が実現できる。

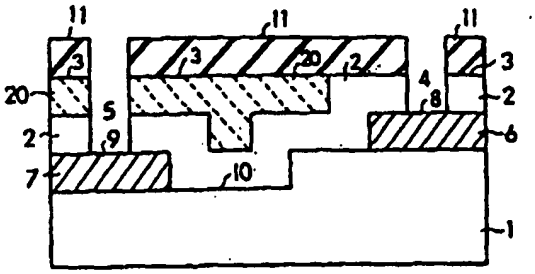
4.図面の簡単な説明

第１図、第２図、および第３図は、本発明の半導体装置の一実施例をしめす断面図、第４図(a)～(h)は、第１図に示した半導体装置の製造方法の一実施例を工程順に示す断面図、第５図(a)～(d)は、第３図に示した半導体装置の製造方法の一実施例を工程順に示す断面図、第６図(a)～(f)は本発明の半導体装置の構成原理を工程順に示す断面図、第７図（Ａ）～（Ｂ）は従来の半導体装置の製造方法の一例を工程順に示す断面図である。

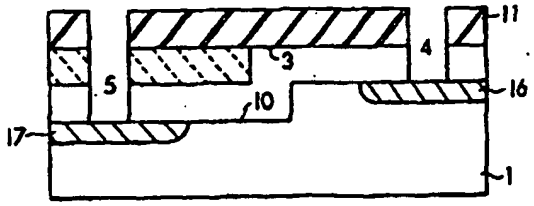
１…半導体デバイスを集積してなる基板

２…絶縁膜

3…最上部絶縁膜の表面
4，5…配線接続穴
6，7…配線
8，9…配線6、7の露出部分
10…基板1の主面
11…ホトレジスト
12…有機高分子材層
13，14…ホトレジスト11の配線接続穴4，5の開口部
16，17…不純物拡散層
20…絶縁膜2とは異なる材質の絶縁膜



第 1 図



第 2 図

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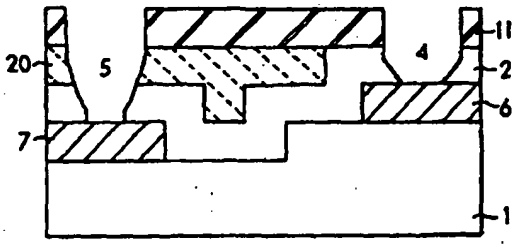
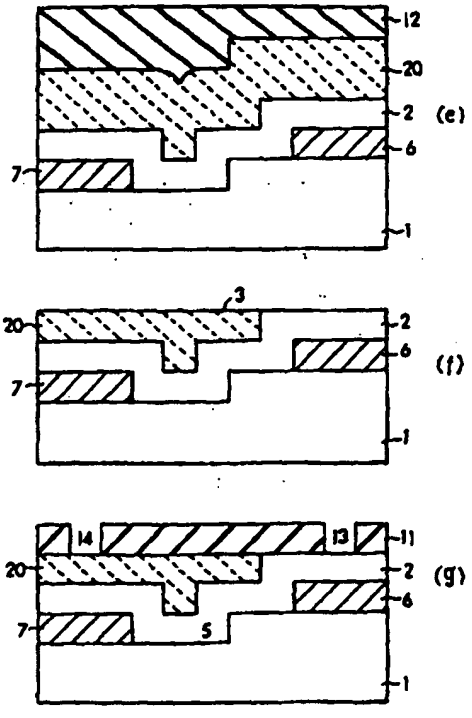
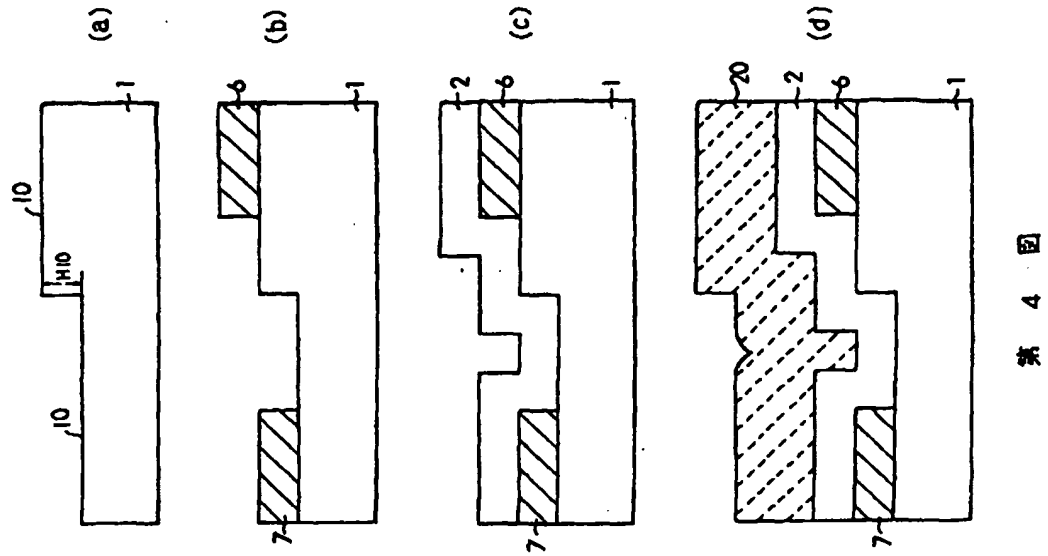
（外2名）



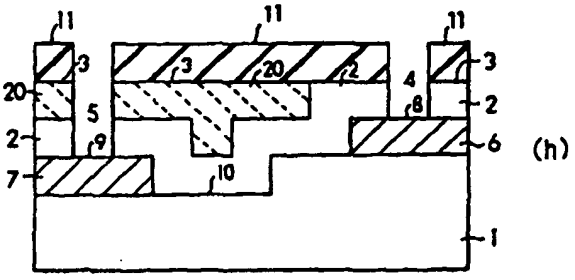
第 3 図



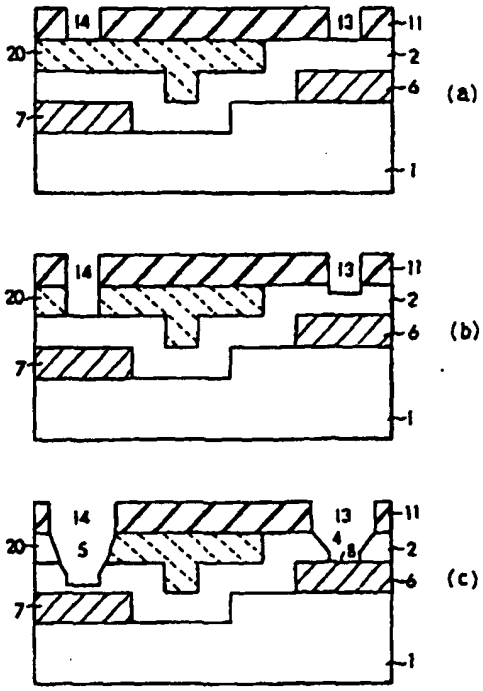
第 4 図



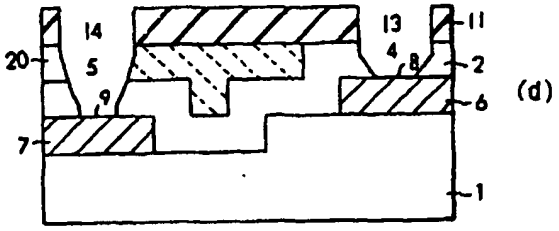
第 4 図



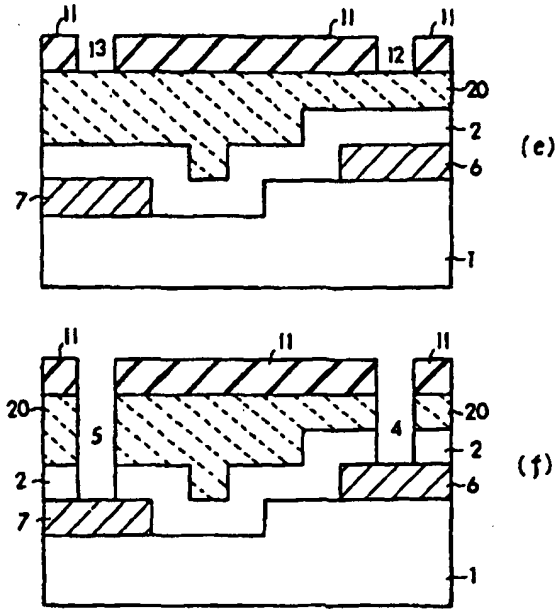
第 4 図



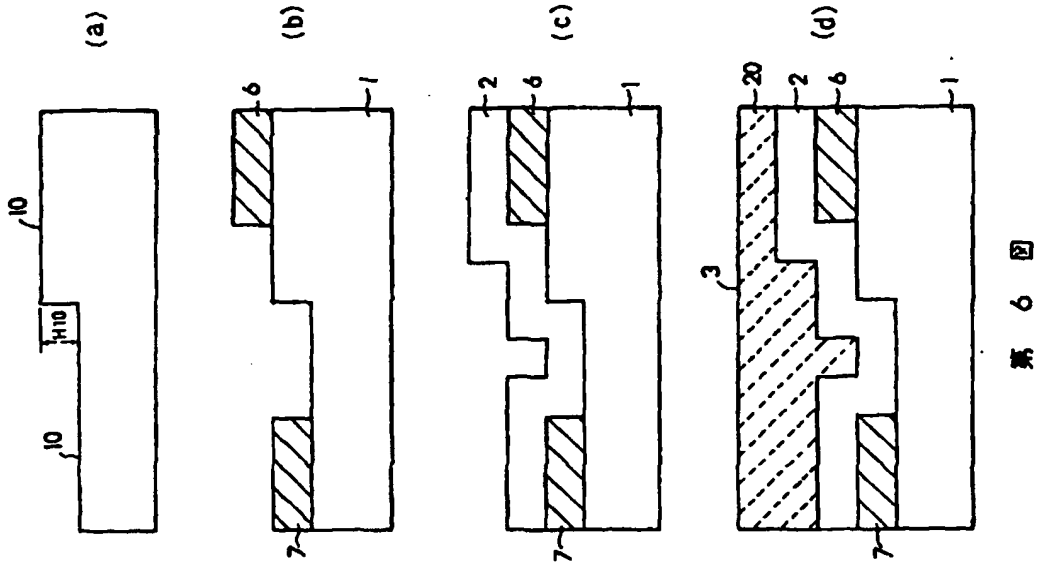
第 5 図



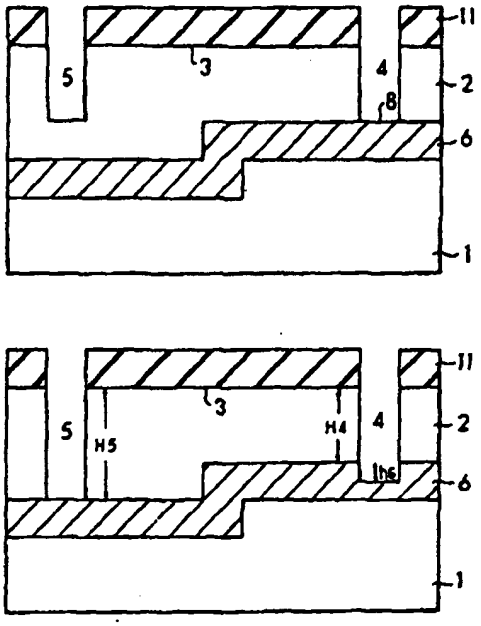
第 5 図



第 6 図



第 6 図



第 7 図

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